SUDHARSHAN SRINIVASAN

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EDUCATION

University of Oregon, Eugene *Sept 2019 - Present*
PhD in Computer Science
Research assistantship supported by Professor Boyana Norris

University of Oregon, Eugene *August 2017 - July 2019*
MS in Computer Science

SRM Institute of Science and Technology, Chennai *July 2013 - May 2017*
BTech in Computer Sceince and Engineering

PUBLICATIONS

- Samuel D. Pollard, **Sudharshan Srinivasan**, and Boyana Norris "A performance and recommendation system for parallel graph processing implementations" in The 10th ACM/SPEC International Conference on Performance Engineering Companion, Mumbai, India, April 2019. ACM
- D.Sundararaman and **Sudharshan Srinivasan** "Twigraph: Discovering and Visualizing Influential Words Between Twitter Profiles" International Conference on Social Informatics. Springer, Cham, 2017.

RESEARCH EXPERIENCE

Performance portability of NUCLEI to GPUs *Jan 2021 - current*

- Writing GPU models on CUDA and HIP that offloads sections of time consuming routines.

Scaling up whole genome simulations *June 2019 - Dec 2020*

- Developed parallel algorithms and implementations in collaboration with MesserLab to scale up SLiM, an evolutionary simulation framework to target multi core CPU clusters.

Selection of parallel graph processing tools *June 2018 - june 2019*

- Implemented a framework for recommending application-specific parallel graph processing toolkits and simplifying necessary build procedure. More details at https://github.com/HPCL/easy-parallel-graph

Ranking sparse linear solvers *Jan 2018 - june 2019*

- Developed an ML based ranking algorithm to select best performing solvers a for target system of linear equations from the PETSc library. More details can be found in my masters thesis

Areas of focus : Distributed systems, asynchronous graph algorithms, code optimization, performance analysis and tuning

WORK EXPERIENCE

Summer internship at Lawrence Livermore National Lab(LLNL) *June'21 - current*

- Implementing routing protocols for YGM, an asynchronous communication library built on top of MPI in C++. Performed experiments for large-scale asynchronous graph algorithms on the Livermore Cluster(LC).

Summer internship at Argonne National Labs(ANL) *June'20*

- Worked on the design of a performance portable library that lets applications using AMD's HIP API to run on devices supporting Intel's level zero specifications. This is part of a larger research project aimed at performance portability of HPC applications to the Aurora supercomputer at ANL

Internship at Tata Consultancy Services *June'17*

- Worked on performance evaluation of the point of sale software used by Target retailers.

TECHNICAL SKILLS

Programming languages: C++(Primary), C, Python
Parallel Programming: MPI, Spark, OpenMP, Intel TBB
GPU programming models: AMD ROCm, Intel oneAPI, CUDA
Performance analysis: Intel VTune Amplifier, Intel Advisor, Caliper, TAU, PAPI,
Compiler toolchain: LLVM, GNU
Machine learning toolkits: PyTorch, SciKit Learn,