Performance Enhancements for HPVM in Multi-Network and Heterogeneous Hardware

- G. Bruno, A. Chien, M. Katz, P. Papadopoulos

Dept. of CSE, U.C.S.D.

INCEP Technologies, San Diego.

A talk by

Sameer Shende,

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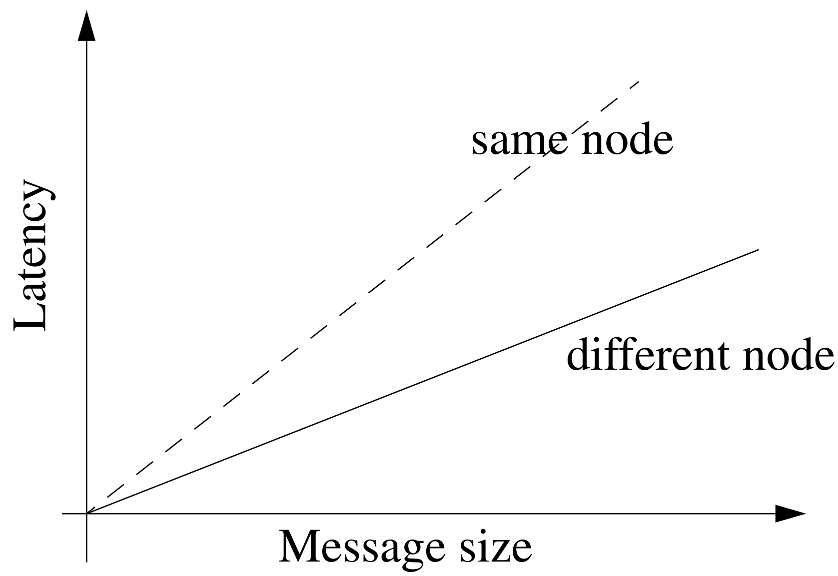
Problems in HPVM

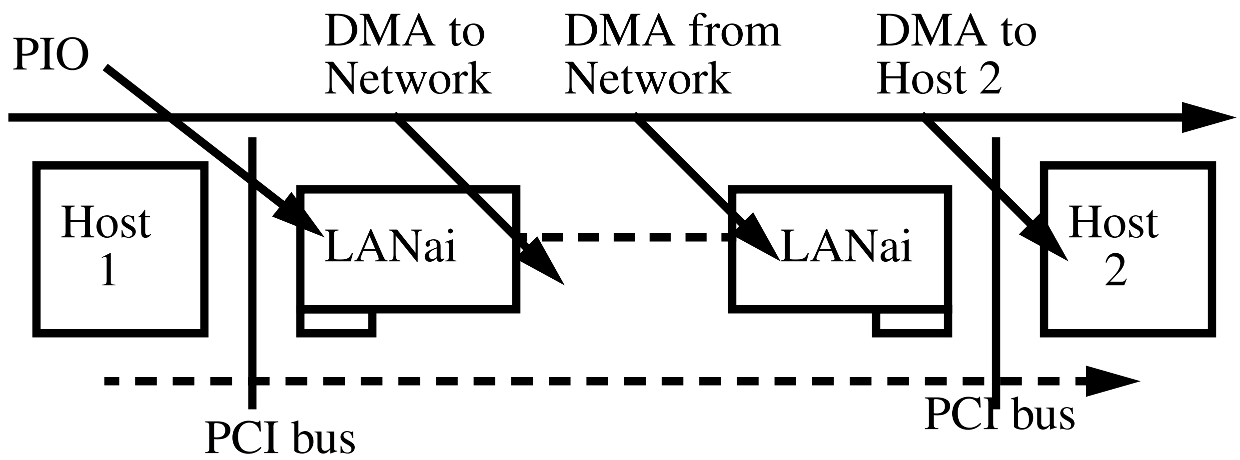
- Used messaging hardware for IPC on same node
  - inter-node performance better than intra-node (for latency, and bandwidth 100MB/s vs 40MB/s).



- New strategy for polling
- Self tuning I/O code to deal with PCI chipset problems

HPVM Design

- ❑ Packets traverse a pipeline



- ❑ LANai NIC
  - ❍ Programmable processor
  - ❍ Software : LCP/MCP (LANai Control Program)
  - ❍ Custom FM LCP
- ❑ DMA: Device driver page-pins memory